REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-12 are currently pending in the present application. Claims 1-3 and 5-7 have been amended and claim 4 has been canceled without prejudice or disclaimer.

II. Claim Amendments

Claim 1 has been amended to recite that the apparatus of claim 1 comprises (i) a chip package, (ii) an integrated circuit electrically connected to the chip package, and (iii) chip logic and a clock tree each disposed on the integrated circuit, where power distributed from a power supply to the chip logic is isolated in the chip package from power distributed from the power supply to the clock tree. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 3 and 4 of the present application.

Claims 2, 3, 5, and 6 have been amended to be consistent with the amendments to claim 1 discussed above. No new matter has been added by way of these amendments.

Claim 7 has been amended to recite that (i) the chip logic operations are conducted on an integrated circuit electrically connected to a chip package, (ii) the clock tree operations are conducted on the integrated circuit, and (iii) the current drawn from the power supply for the chip logic operations is isolated in the chip package from the

current drawn from the power supply for the clock tree operations. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 3 and 4 of the present application.

III. Objection(s) to the Claims

Claim 4 was objected to as not further limiting the subject matter of the claim from which it solely depends. By way of this reply, claim 4 has been canceled, and thus, the objection to claim 4 is now moot. Accordingly, withdrawal of the objection to claim 4 is respectfully requested.

IV. Rejection(s) Under 35 U.S.C § 103

Claims 1-12 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,172,330 issued to Watanabe et al. (hereinafter "Watanabe"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for reducing clock skew and/or noise by isolating a power supply distribution between a clock tree and chip logic. With reference to the exemplary embodiment of the present invention shown in Figure 4 of the present application, power distributed from a power supply **94** to a clock tree **62** (disposed on an integrated circuit **60** electrically connected to a chip package **100**) is isolated in the chip package **100** from power distributed from the power supply **94** to chip logic **64**. *See* Specification, paragraph [0016].

Accordingly, amended independent claim 1 of the present application requires, in part, that power distributed from the power supply to the clock tree *is isolated in the chip*

package from power distributed from the power supply to the chip logic. Further, amended independent claim 7 of the present application requires, in part, that the current drawn from the power supply for the chip logic operations *is isolated in the chip package* from the current drawn from the power supply for the clock tree operations. The isolation of power or current draw in the chip package leads to additional benefits such as, for example, increased reduction in clock skew and/or noise.

Watanabe, on the other hand, fails to disclose at least those limitations of the claimed invention discussed above. Watanabe is directed to an integrated circuit in which the layout design of a clock supplying circuit of the integrated circuit can be started independently of the layout design of a logic circuit area of the integrated circuit. *See* Watanabe, column 1, lines 6 – 11. In Figure 12 of Watanabe, which is relied upon by the Examiner, "power source lines **1201** for a logic circuit area **124** are separated from power source lines **1202** for a clock buffer **1205** on an integrated circuit substrate." *See* Watanabe, column 4, lines 24 – 28. However, both the figures and text of Watanabe are completely silent as to isolating power and/or current draw distribution *in a chip package* as required by amended independent claims 1 and 7 of the present application. In fact, Watanabe is altogether silent as to a chip package. Those skilled in the art will recognize that a chip package and an integrated circuit substrate are distinct components with different properties, functions, and characteristics. Accordingly, Watanabe necessarily cannot and does not disclose the limitations of the claimed invention discussed above.

In view of the above, Watanabe fails to show or suggest the present invention as recited in amended independent claims 1 and 7 of the present application. Thus, amended independent claims 1 and 7 of the present application are patentable over

Watanabe. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.114001; P6325).

Respectfully submitted,

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